

## REMARKS

Claims 1-13 are pending and claims 1-7 stand rejected. Applicants gratefully acknowledge that claims 8-13 are allowed. Claims 1-7 have been amended to particularly point out and distinctly define the present invention over the prior art of record. Support for the amendments may be found at least in the FIGS. And specification as originally filed.

Claims 1-13 are pending and under consideration. Reconsideration is respectfully requested. No new matter has been added.

### **102(e) rejection of claims 1-5 and 7:**

Claims 1-5 and 7 were rejected under 35 U.S.C. 102(e) as being anticipated by Yamamoto et al. (U.S. Patent No. 6,724,359); and claims 1 and 2 were rejected under 35 U.S.C. 102(e) as being anticipated by Lee (U.S. Patent No. 6,760,082). The foregoing rejections are respectfully traversed.

Regarding the Yamamoto reference:

The Applicants respectfully submit that Yamamoto fails to disclose the all of the features as recited in claim 1, for example. Specifically, Yamamoto fails to teach the Applicants “a first thin film transistor...a pair of first and second pixel electrodes capacitively coupled to each other, disposed on the pixel areas defined by intersections of the gate lines and data lines; and a *second thin film transistor connected to the second pixel electrode and one of the first gate lines that is disconnected from the first thin film transistor,*” as recited in claim 1, for example.

In contrast, in FIGS. 1 and 2, Yamamoto discloses a LCD device 100 which includes a plurality of LC capacitors 10, a plurality of storage capacitors 20 each storage capacitor including a pixel electrode 12, a counter electrode 16 opposing the pixel electrode (see column 5, lines 30-45, for example). Further, Yamamoto discloses that each storage capacitor 20 includes a storage capacitor electrode 22 electronically connected to the pixel electrode 12, a storage capacitor counter electrode 26 opposing the storage capacitor electrode 22, and a gate insulating film between the storage capacitor electrode 22 and the storage capacitor counter electrode 26. The LCD device 100 further includes a TFT substrate which includes a first, second and third TFT 30, 40 and 50 formed on an insulative substrate, scanning lines and a signal line, and a reference line connected to the first, second and third TFTs 30, 40 and 50 (see column 6, lines 37-43, for example).

At page 3 of the Office Action, regarding claim 1, the Examiner asserts that the “storage

capacitor counter electrode 26” of Yamamoto is comparable to the Applicants “first pixel electrodes”; the second TFT 40” of Yamamoto is comparable to the Applicants “first thin film transistors”; and “the storage capacitor electrode 22” of Yamamoto is comparable to the Applicants “second pixel electrodes”; and the “first TFT 30” of Yamamoto is comparable to the Applicants “second thin film transistors”. The Applicants respectfully disagree with the Examiner. The Applicants respectfully submit that the storage capacitor electrode 26 of Yamamoto is not equivalent to the Applicants “first pixel electrodes”. Thus, the second TFT 40 of Yamamoto does not include “**a first thin film transistor connected to one of the gate lines and one of the data lines, and connected to or capacitively coupled to the first pixel**” as recited in claim 1, for example. Further, the storage capacitor electrode 22 of Yamamoto is not equivalent to the Applicants “second pixel electrode”. Thus, the first TFT 30 of Yamamoto (see FIGS. 10 and 11) does not include “a second thin film transistor connected to the second pixel electrode and one of the gate lines that is disconnected from the first thin film transistor” as recited in claim 1. Thus, the present invention as recited in claim 1, for example, patentably distinguishes over Yamamoto.

Regarding the Lee reference:

Like Yamamoto, the Applicant respectfully submits that Lee also fails to discuss the Applicants “second thin film transistors”

In contrast, Lee discloses at FIG. 4B, a pixel unit of TFT array substrate, the pixel unit includes at least two pixels A and B each pixel having a TFT 230, a first floating electrode 260, a second floating electrode 270, and a pixel electrode 240. The TFT 230 is disposed on a scanning line 210, and includes a source/drain electrode 232 and a gate electrode 234. The first floating electrode 260 and the second floating electrode 270 are formed on the pixels (A and B) and parallel to the signal lines 220). The pixel electrode 240 is formed partially overlapping the first floating electrode 260 and the second floating electrode 270, and is electrically connected to the TFT 30 by a contact hole (see column 3, lines 20-47, for example). As shown in FIG. 4B, the TFT 230 in pixel B does not include “a second thin film transistor connected to the second pixel electrode and one of the gate lines that is disconnected from the first thin film transistor. Thus, the present invention as recited in claim 1, for example, patentably distinguishes over Lee.

**103(a) rejection of claim 6:**

Claim 6 was rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto in view of Kim et al. (U.S. Patent No. 6,473,142). The foregoing rejection is respectfully traversed.

Based upon the comments mentioned above, Yamamoto fails to disclose all of the features of claim 1 from which dependent claim 6 directly depends. Thus, although Kim discloses a multi-domain LCD device where the multi-domain is obtained by dividing each pixel

into four domains, for example (see column 6, lines 1-4), Kim fails to make up for the deficiencies of Yamamoto as mentioned above.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or discuss all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See M.P.E.P. § 2142.

Therefore, the combination of the foregoing references fails to provide a *prima facie* case of obviousness over the present invention.

Thus, withdrawal of the rejection is respectfully requested.

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

Applicants hereby petition for any necessary extension of time required under 37 C.F.R. 1.136(a) or 1.136(b) which may be required for entry and consideration of the present Reply.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 06-1130.

Respectfully submitted,

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By: /James J. Merrick/

James J. Merrick  
Registration No. 43,801  
Cantor Colburn LLP  
20 Church Street, 22<sup>nd</sup> Floor  
Hartford, CT 06103-3207  
Telephone: (860)286-2929  
Facsimile: (860)286-0115